

Form PTO-1449 (Modified)  
(Rev. 11/92)U.S. Dept. of Commerce  
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ATTY. DOCKET NO.

SERIAL NO.

0254-094-CIP4-C1

10/814,530

## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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APPLICANT

Rapport, et al

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3/31/04

GROUP 2822

## U.S. PATENT DOCUMENTS

*Examiner Initial	Patent Number		Patentee	Class	Subclass	Filing Date (if appropriate)
TYT	5,428,190	6/27/1995	Stopperan	174/261		7/2/1993
	6,097,087	8/1/2000	Farnworth, Warren M. et al	257/698		10/31/1997
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	6,444,921B1	9/3/2002	Wang, et al	174/260		2/3/2000
	6,465,877B1	10/15/2002	Farnworth, Warren M. et al	257/668		3/27/2000
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	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
TYT	58-96756(A)	06/08/1983	Japan	—	—	Partial	
	58-112348(A)	07/04/1983	Japan	—	—	Partial	
	60-254762	12/1985	Japan	—	—	Partial	
	EP 0 298 211 A#	01/11/1989	European	—	—	X	

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TYT	Dense-Pac Microsystems, Breaking Space Barriers, 3-D Technology 1993
TYT	Dense-Pac Microsystems, DPS512X16A3, Ceramic 512K X 16 CMOS SRAM Module
TYT	"Design Techniques for Ball Grid Arrays," William R. Newberry, Xynetix Design Systems, Inc.

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	6,300,679 B1	10/9/2001	Mukerji et al.	257/738		6/1/1998
	6,462,412 B2	10/8/2002	Kamei et al	257/723		1/17/2001
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	6,486,544 B1	11/26/2002	Hashimoto, Nobuaki	257/686		9/3/1999
	6,560,117 B2	5/6/2003	Moon, Ow Chee	361/749		8/30/2001
	6,590,282 B1	7/8/2003	Wang et al.	257/686		4/12/2002
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						Yes	No
TYT	62-230027(A)	10/08/1987	Japan			Partial	

**OTHER DOCUMENTS**

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TYT	"Chip Scale Packaging and Redistribution," Paul A. Magill, Glenn A. Rinne, J. Daniel Mis, Wayne C. Machon, Joseph W. Baggs, Unitive Electronics Inc.
TYT	"3D Interconnection for Ultra-Dense Multichip Modules," Christian VAL, Thomson-CSF DCS Computer Division, Thierry Lemoine, Thomson-CSF RCM Radar Countermeasures Division
TYT	"High Density Memory Packaging Technology High Speed Imaging Applications," Dean Frew, Texas Instruments Incorporated
TYT	Teresa Technologies, Inc. - Semiconductor Intellectual Property, Chip Scale Packaging - Website pages (3)

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TTT	6,473,308B2	10/29/2002	Forthun	361/749		04/19/2001
	US2002/0006032A1	01/17/2002	Karabatsos	361/760		01/11/2001
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**OTHER DOCUMENTS**

(INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

TTT	"Tessera Introduces uZ™ - Ball Stacked Memory Package for Computing and Portable Electronic Products" Joyce Smaragdis, Tessera Public Relations; 2 figures that purport to be directed to the uZ™ - Ball Stacked Memory Package.
TTT	Ron Bauer, Intel. "Stacked-CSP Delivers Flexibility, Reliability, and Space-Saving Capabilities", Spring 2002.
TTT	Tessera uZ Ball Stack Package. 4 figures that purport to be directed to the uZ - Ball Stacked Memory, 1 Page.
TTT	"Vertically-Integrated Package," Alvin Weinberg, Pacesetter, Inc. and W. Kinzy Jones, Florida International University

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TYT	6,620,651B2	9/16/2003	He et al.	438/113		10/23/2001
	US2002/0139577A1	10/3/2002	Miller, Charles A.	174/261		3/27/2001
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	US2002/0180022A1	12/5/2002	Emoto, Yoshiaki	257/686		7/19/2002
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	3,772,776	11/20/1973	Weisenburger	29/628		12/03/1969
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	4,911,643	03/27/1990	Perry, et al	439/67		08/03/1989
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	4,956,694	09/11/1990	Eide	357/74		11/04/1988
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**OTHER DOCUMENTS**

(INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

TYT	Dense-Pac Microsystems, 256 Megabyte CMOS DRAM DP3ED32MS72RW5
TYT	IBM Preliminary 168 Pin SDRAM Registered DIMM Functional Description & Timing Diagrams

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	5,138,430	08/11/1992	Gow, 3 <sup>rd</sup> , et al	357/70		06/06/1991
	5,159,434	10/27/1992	Kohno, et al	357/80		02/01/1991
	5,222,014	06/22/1993	Lin	361/414		03/02/1992
	5,224,023	06/29/1993	Smith, et al.	361/412		02/10/1992
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	5,281,852	01/25/1994	Normington	257/685		12/10/1991
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	5,572,065	11/05/1996	Burns	257/666		10/24/1994
	5,612,570	03/18/1997	Eide, et al	257/686		04/13/1995
	5,644,161	07/01/1997	Burns	257/668		06/07/1995
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TYT	5,778,552	7/14/1998	LeGuin	33/559		5/8/1996
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	6,208,521B1	3/27/2001	Nakatsuka	361/749		5/19/1998
	6,225,688B1	05/01/2001	Kim et al.	257/686		02/04/1999
	6,281,577B1	08/28/2001	Oppermann et al.	257/724		04/22/1997
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